Address Map		
CPU	**Leon3**	**Ariane/Ibex**
Main Memory (1GB)	0x40000000 - 0x7FFFFFFF	0x80000000 - 0xBFFFFFFF
I/O and registers (256 MB)	0x80000000 - 0x8FFFFFFF	0x60000000 - 0x6FFFFFFF
Bootrom (128KB)	0x00000000 - 0x0001FFFF	0x00000000 - 0x0001FFFF
Frame buffer (512KB)	0x30100000 - 0x3017FFFF	0x30100000 - 0x3017FFFF
RISC-V CLINT (768KB)	n/a	0x02000000 - 0x020BFFFF
SLM scratchpad (64MB)	0x04000000 - 0x07FFFFFF	0x04000000 - 0x07FFFFFF
LPDDR scratchpad (1GB) - GF12 only	0xC0000000 - 0xFEFFFFFF	0xC0000000 - 0xFFFFFFFF
Leon3 AHB device tree area (16MB)	0xFF000000 - 0xFFFFFFFF	n/a

Address Map of I/O and Registers			
Core	**APB base address**		
Leon3	80000000		
Ariane/Ibex	60000000		
Standard APB Device	**APB start offset**	**APB end offset**	**APB index**
UART	000 001 00	000 001 FF	1
L3 IRQ controller**	000 002 00	000 002 FF	2
L3 timer	000 003 00	000 003 FF	3
ESPLink	000 004 00	000 004 FF	4
SVGA	000 006 00	000 006 FF	13
SGMII PHY	000 010 00	000 01F FF	15
CPU0 DVFS	000 0D5 00	000 0D5 FF	5
CPU1 DVFS	000 0D6 00	000 0D6 FF	6
CPU2 DVFS	000 0D7 00	000 0D7 FF	7
CPU3 DVFS	000 0D8 00	000 0D8 FF	8
CPU0 L2	000 0D9 00	000 0D9 FF	9
CPU1 L2	000 0DA 00	000 0DA FF	10
CPU2 L2	000 0DB 00	000 0DB FF	11
CPU3 L2	000 0DC 00	000 0DC FF	12
MEM0 LLC	000 0E0 00	000 0E0 FF	16
MEM1 LLC	000 0E1 00	000 0E1 FF	17
MEM2 LLC	000 0E2 00	000 0E2 FF	18
MEM3 LLC	000 0E3 00	000 0E3 FF	19
Partial-reconf controller (PRC)	000 0E4 00	000 0E4 FF	127
ESP ACC0*** (32 registers)	000 100 00	000 100 7F	84
ESP ACC0 DVFS (32 registers)	000 100 80	000 100 FF	84
*... up to 42 ESP accelerators****			85-125

ESP ACC42 (32 registers)	000 12A 00	000 12A 7F	126
ESP ACC42 DVFS (32 registers)	000 12A 80	000 12A FF	126
GRETH MAC	000 800 00	000 8FF FF	14
TILE0 monitor (128 registers)	000 900 00	000 901 FF	20
... up to 64 tiles			21-82
TILE63 monitor (128 registers)	000 97E 00	000 97F FF	83
APB controller reserved	**APB start offset**	**APB end offset**	**APB index**
Leon3 APB PnP table	000 FF0 00	000 FFF FF	n/a
Device w/ extended APB address*	**APB start offset**	**APB end offset**	**APB index**
Third-party ACC0***	004 000 00	004 FFF FF	84
*... up to 44 third-party accelerators***			85-126
Third-party ACC43***	02F 000 00	02F FFF FF	127
RISC-V PLIC**	0C0 000 00	0FF FFF FF	2
Notes			
* Leon3 device tree generation w/ *mklinuximg* is not currently supporting discovery of these devices			
** L3 IRQ controller and RISC-V PLIC are never present in the same ESP instance.			
*** The accelerator ID is dynamically assigned based on the ESP configuration file. The ID assignment is based purely on the tile placement, not on the type of accelerator (ESP or third-party).			
**** At this time we can have up to 44 accelerators (ESP + third-party), but we can easily extend this limit to 172 (428) by allowing the APB bus to handle up to 256 (512) slaves.			